

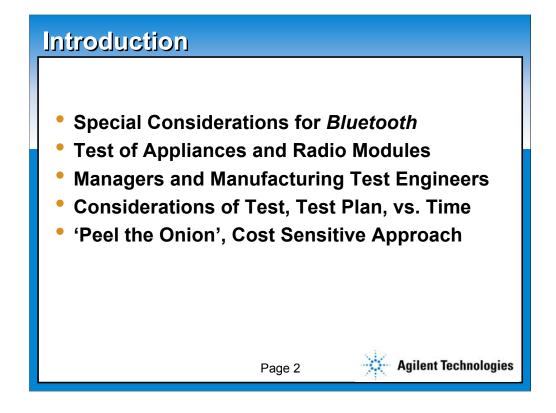
## Bluetooth<sup>™</sup> Manufacturing Test

#### April 23, 2002

presented by:

### **Brian Fetz**

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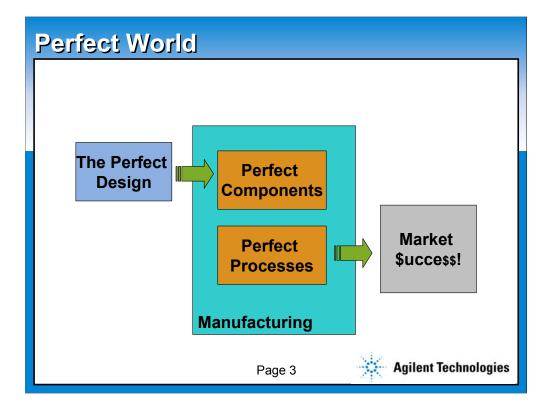
This presentation is focused on the manufacturing test requirements for Bluetooth enabled appliances as well as for the Bluetooth modules that may be used for enabling such appliances.

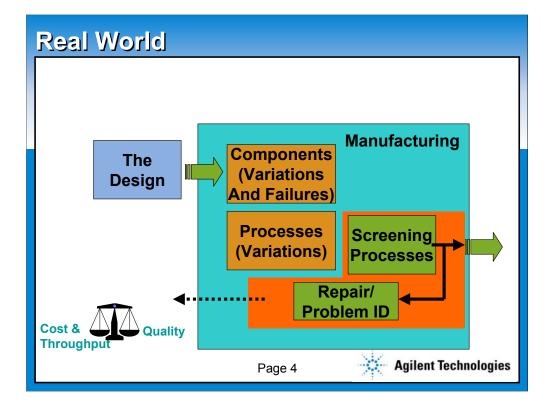
It is of particular interest for manufacturing test engineers and manufacturing managers who have responsibility for such appliances and modules. Though the presentation is focused on manufacturing of the higher level components of Bluetooth enabled products, it will also be of interest to Bluetooth IC vendors as there are many things that are said about them and how they and their products influence the direction one may take.

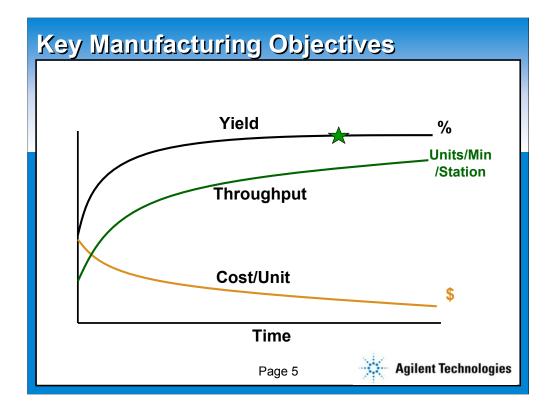
Much has been written about Bluetooth testing and what has falls into largely two categories---detailed write-ups describing particular tests and their equipment needs and those that are fairly superficial that suggest one should test and that one should select tests wisely. Little guidance is given on picking the methodology of a test or even how best to know you should. I aim to deliver on an approach that if followed will go through an exhaustive consideration of test, AND ultimately be sued to synthesize a test plan, and furthermore, show briefly how that test plan may change over time.

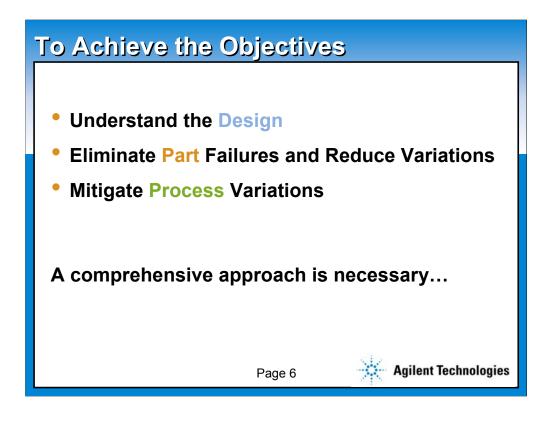
Is Bluetooth special? Yes---it is an RF technology and it is supposed to be low cost with low power consumption AND there are a myriad of products and philosophies of those making those products.

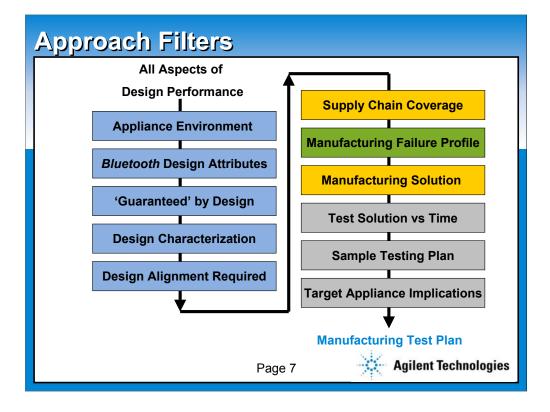
The presentation today will be a 'peel the onion' approach to deriving the test plan--- we will start at a fairly high level that most of us will agree upon, and dig down through the many layers that have to be considered---In this approach, one will see that it is a cost sensitive approach which is something most of us are concerned about.

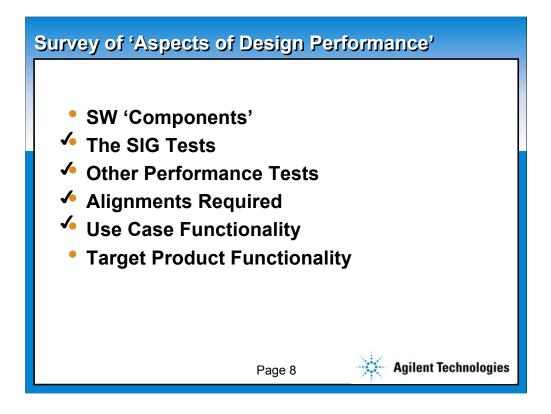


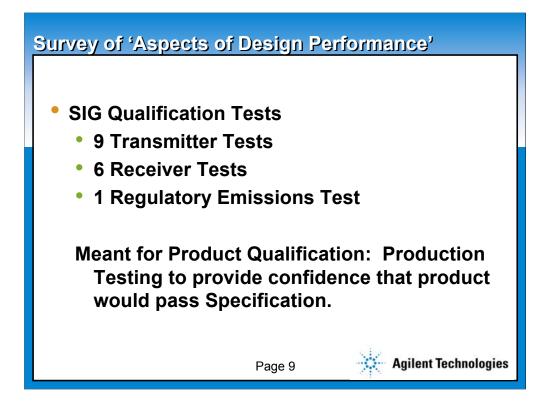


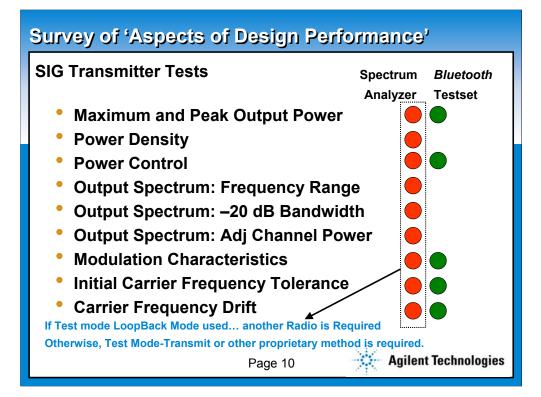


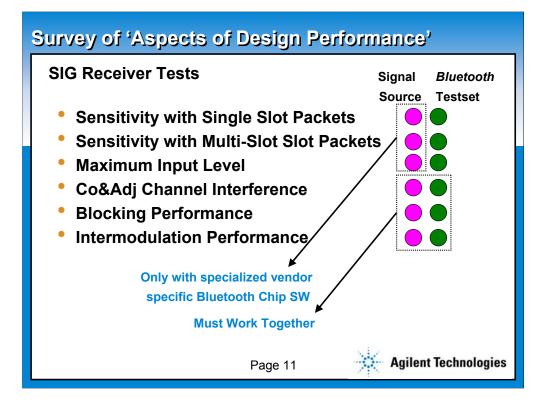


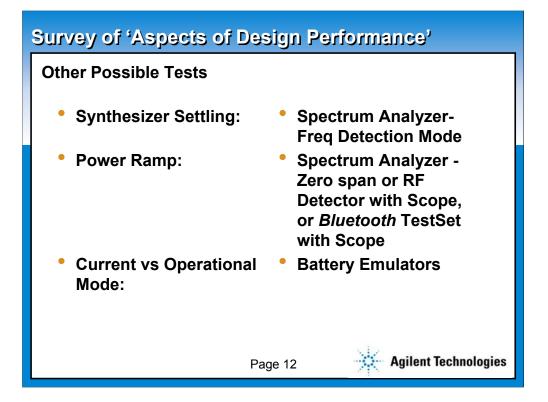


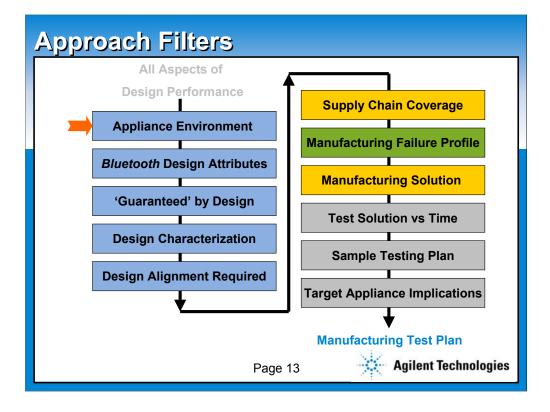


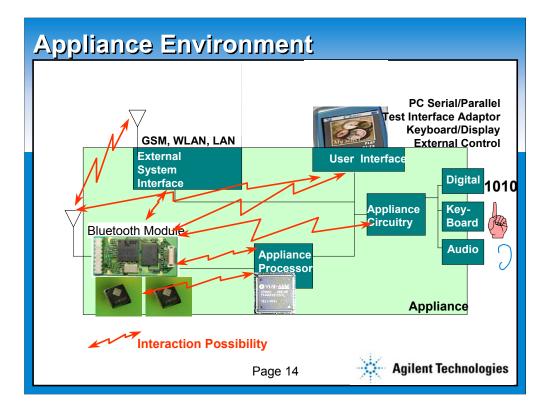


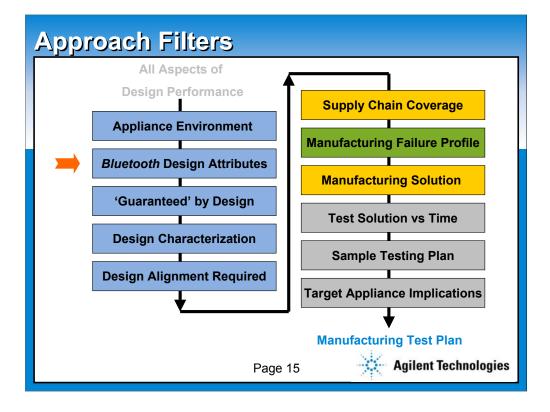


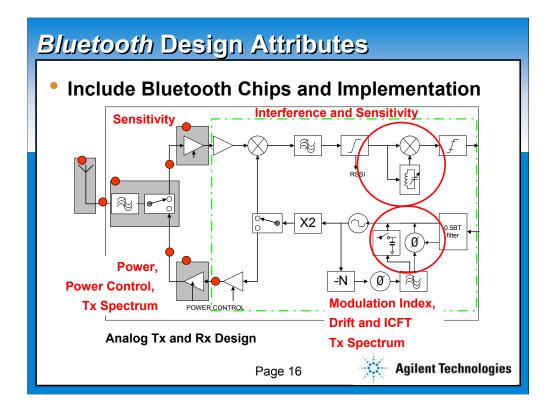






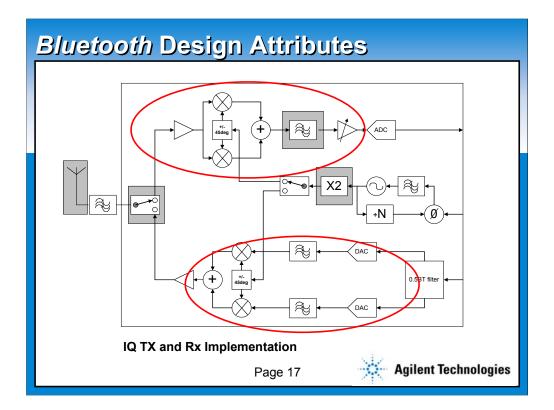


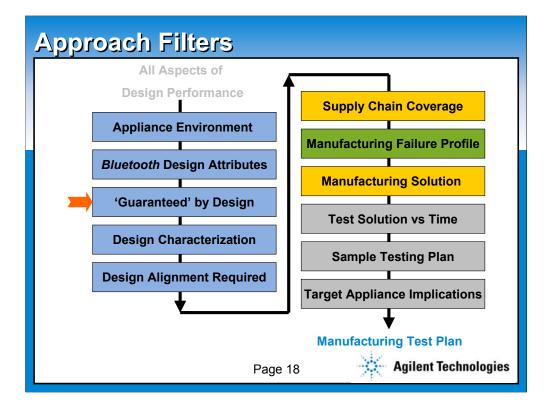


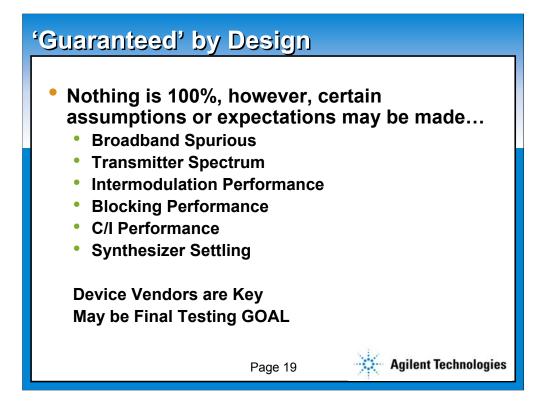


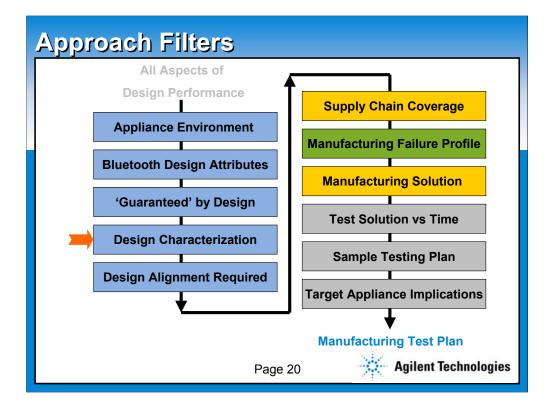
This diagram shows quite a bit of information, but there are three main areas to focus upon:

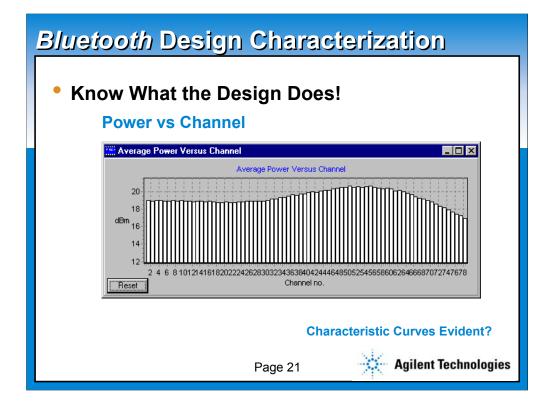
- 1. Block Diagram of Design
- 2. Radio Partitioning—multi-ic or not. Locating the boundaries over which the specifications can be made
- 3. Process susceptibilities in the assembly of the radio
- In this diagram we see a direct modulation of a vco for the transmitter. These were probably the original expected implementation and these can have certain tendencies in performance. In those cases where the loop is opened during the transmit cycle, these can drift substantially and may have characteristics that change over frequency.
- The red dots indicate issues in partitioning of the design. When different components are used—there are different interfaces which all increase likelihood of failure or extreme variation.
- Of particular note that over the partitioning, the various parameters are affected differently. For instance, Sensitivity and Power Out parameters are dependent on absolute levels (in and out). Modulation characteristics are dependent on the Bluetooth transmitter alone (assuming no regulation issues). A Tx Spectrum performance may be split over the Bluetooth transmitter as well as the power amp IC (which may cause distortion)

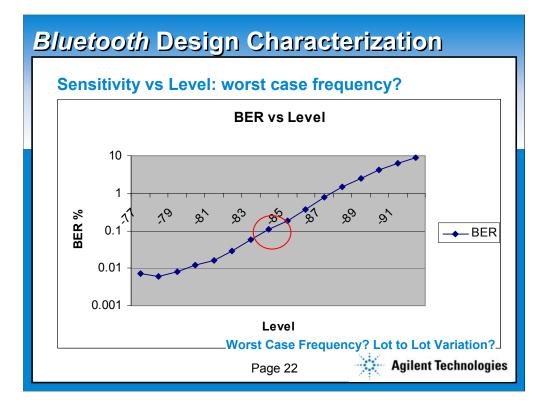


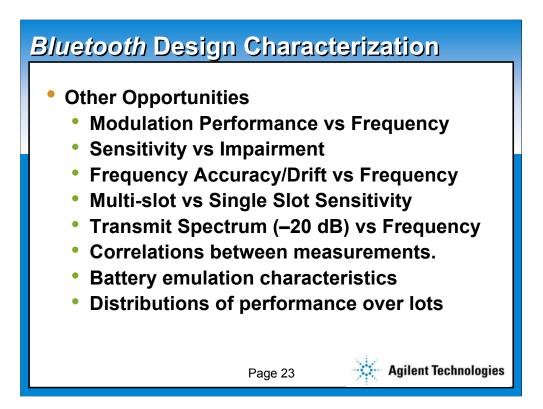


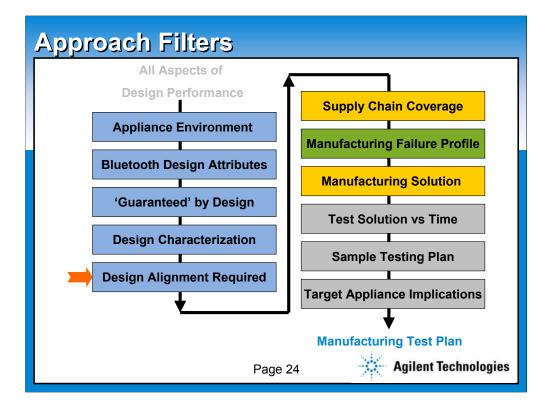


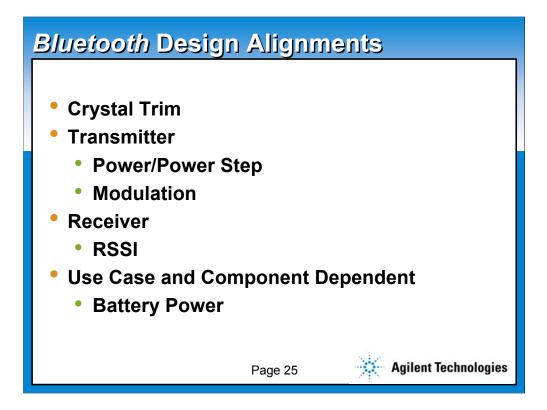


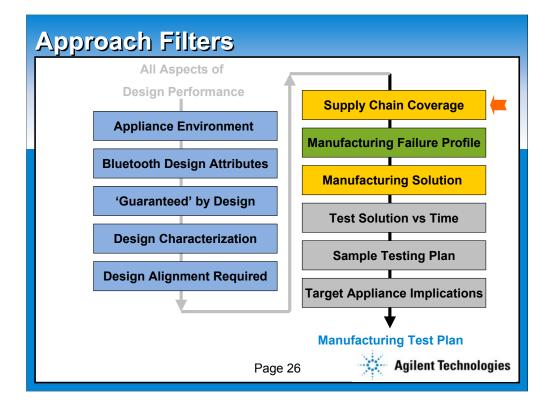












### Supply Chain Test Coverage

- Examine the Test Coverage of *Bluetooth* Vendors IC and Module Vendor (if appropriate).
- Understand Methodology Differences– they are testing physical parameters mostly.
- Discern Correlation with your implementation
- Create a Coverage Table/Matrix

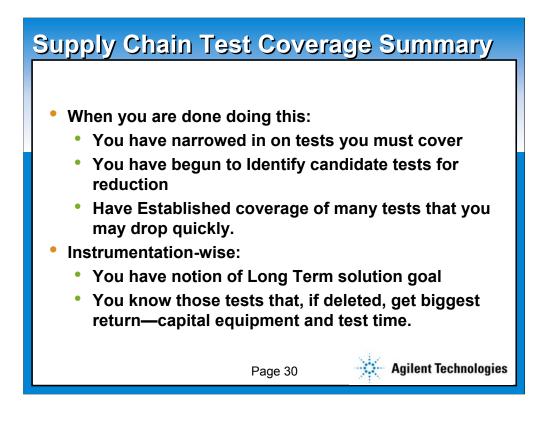
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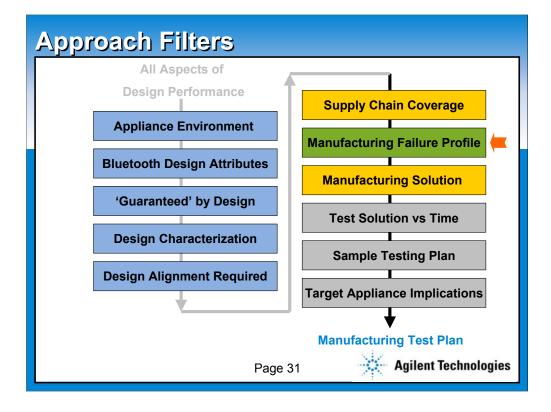
**Agilent Technologies** 

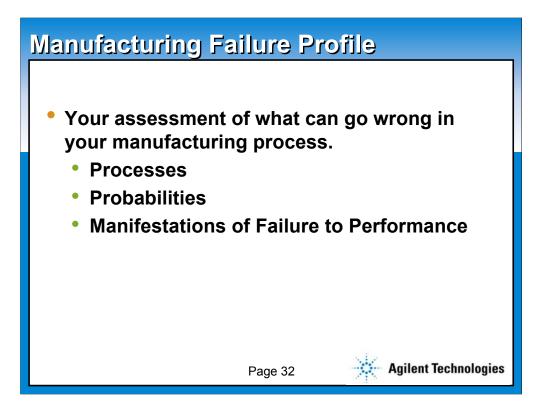
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ooverage matrix			IC -	Test											-	-			
	letien:		Power vs Freq	Control		Spurious Signal Generation: IB	Spurious Signal Generation: OB	Frequency Settling Time	Mod Char:Modulation Index	Mod Char:Initial Frequency Accuracy	Mod Char:Frequency Drift	Rx Intermodulation Distortion	Rx Interference: Blocking	Rx Interference: Co Channel	Rx Interference: Adj Channel	Dynamic Range:Sensitivity	Dynamic Range:Max Input Power	Tests	
Strong Corre				ver (		igna	igna	Settl	Modu	Initia	Frequ	dula	ence	ence	ence	ic Ra	ic Ra	and DC.	
Weak Correla	tion	lent	Output	ΡO	ΒW	us S	us S	ency:	har:I	har:I	har:f	emc	erfen	erfen	erfen	nami	nami	and	
Alignment Re	equired	Alignment	Max C	Output Power	20 dB BW	purio	purio	edue	od C	od C	od C	x Inte	x Inte	x Int	x Inte	Rx Dy	Rx Dy	Digital a	
Alignment Tests		∢	Σ	0	2	S	S	ш	Σ	Σ	Σ	Я	Ж	Я	Я	Я	Я	Δ	
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	Power Output	Y	х																
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	Carrier Frequency Drift	Ν									Х								
	Sensitivity	Ν														х			
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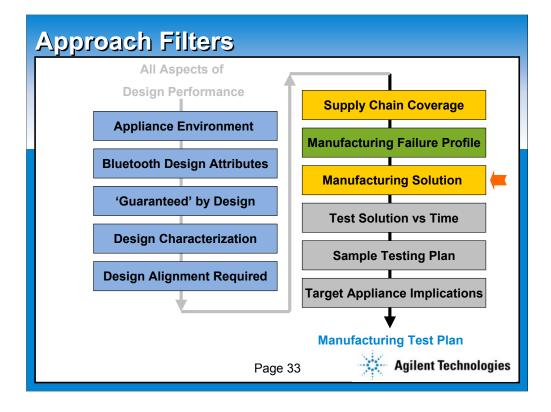
# Supply Chain Test Coverage

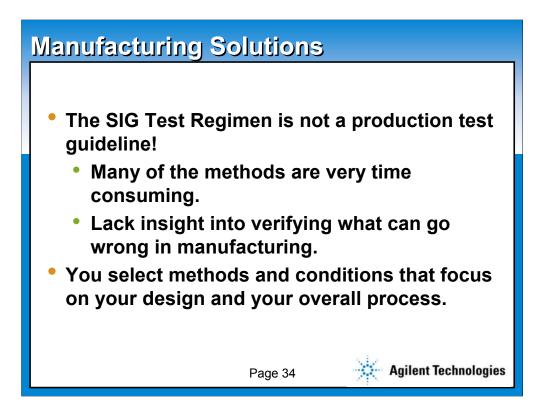
Coverage Matrix	cont		Ups	strea	am T	Fests	s in f	the \$	Supp	oly C	Chai	n							
ooverage matrix		IC <sup>-</sup>	Test																
Strong Correl		Alignment	Max Output Power vs Freq	Output Power Control	20 dB BW	Spurious Signal Generation:IB	Spurious Signal Generation:OB	FrequencySettling Time	Mod Char:Modulation Index	Mod Char:Initial Frequency Accuracy	Mod Char:Frequency Drift	Rx Intermodulation Distortion	Rx Interference:Blocking	Rx Interference:Co Channel	Rx Interference:Adj Channel	Rx Dynamic Range:Sensitivity	Rx Dynamic Range:Max Input Power	Digital and DC Tests	
Other SIG Tests	Marries and Landala Land		2	0	Ñ	S	S	ш	2	2	2	Я	Я	Я	Ж	ц			
Other SIG Tests		N N	-	-	-		V										х		
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	Carrier/Interference Performance						х							×				_	
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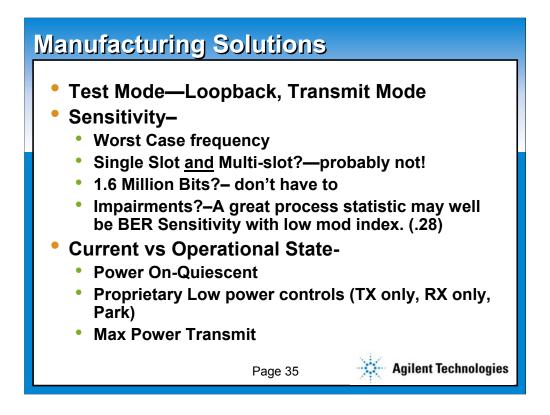










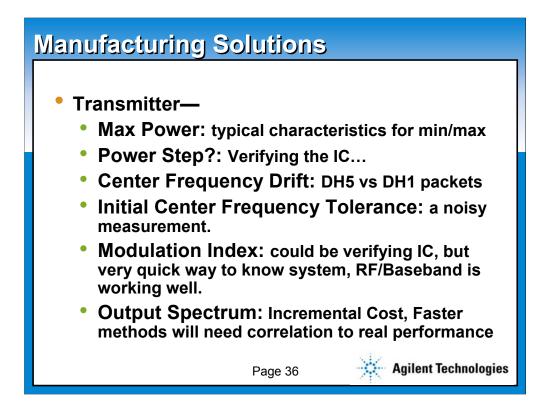


In selecting the tests to do you can use the facilities of the Test mode modes loopback and transmit modes as well as perhaps proprietary BER Receive modes.

With respect to testing Sensitivity it is very likely that both multi-slot and single slot testing is unnecessary---find the worst case, (multi-slot), and omit the other. Further, the number of bits (1.6 Million) can be adequately done at substantially fewer bits. Testing to a spec of .07% at 30,000 bits or .082 at 100,000 bits.

I feel that in manufacturing impairments as a suite are not particularly useful. Generally, in Manufacturing we want the stimulus to be as pure as possible to keep the margins high. If there is reason to believe that there is an ongoing issue with performance (say a Symbol timing Recovery circuit) that can be a function of silicon and is found only with a special condition then set that condition up---For example, set up the modulation index to be at the low end and the frequency offset to be either at the high or low extreme.

Current draw, as stated earlier, may be an incredibly simple measurement to make that actually yields great benefits in identify things that might go wrong. It may be that a very narrow distribution should exist for any particular operating mode and that a significant deviation from this would indicate poor silicon characteristics, soldering defects, component failure, etc



For the transmitter, we can make some simplifications depending on what we have learned through the approach to this point:

Max Power—what are the characteristics vs frequency? Pick only key areas of variability or where spec margin is low.

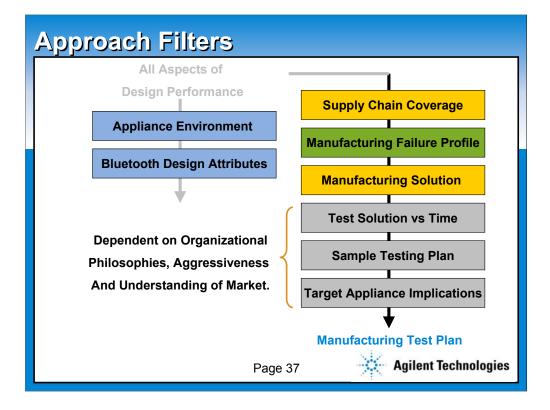
Power Step-if this is not a calibrated parameter—this would be essentially verifying the IC which may well have been done at the IC vendor.

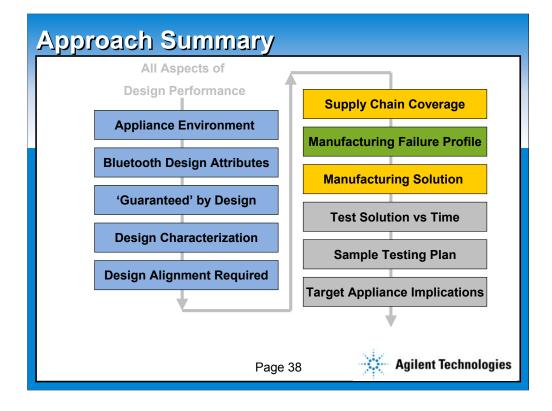
Center Frequency Drift—choose only one packet type, if appropriate.

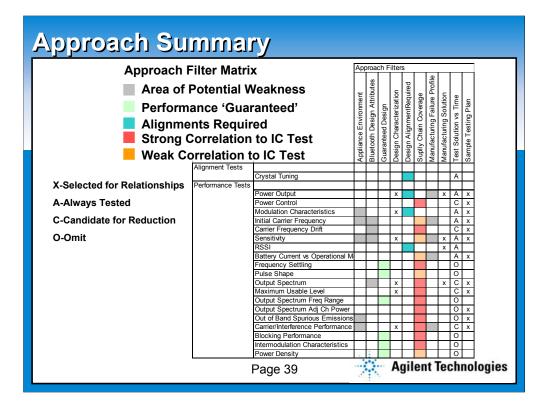
Initial Frequency Tolerance---realize that this is a noisy measurement.

Modulation Index---realize that you could be verifying the IC—however, is an efficient means to gain confidence in the baseband and RF IC connection.

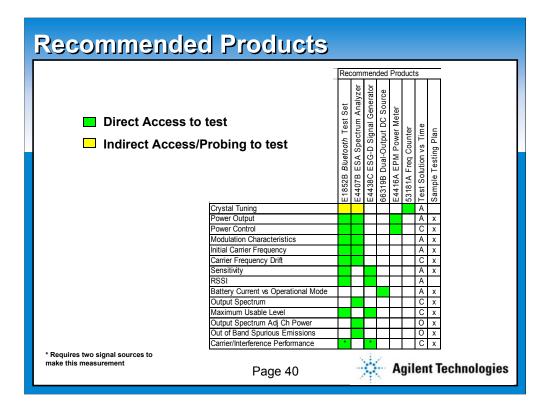
Output Spectrum: could be a function of environment. If not, may be just testing the IC for physical parameters that the IC vendor may have already determined in their tests

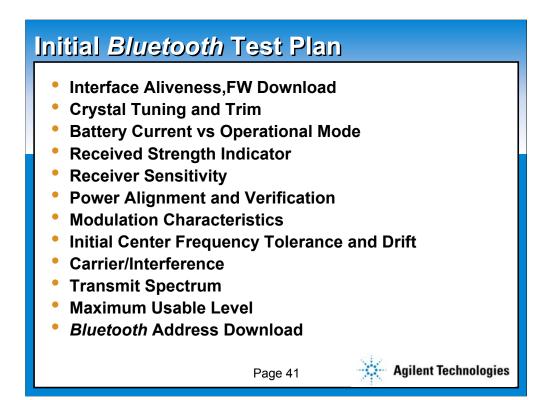




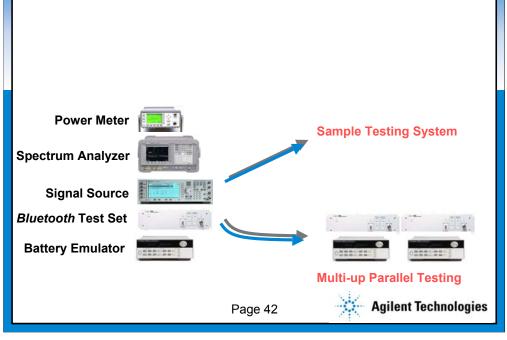


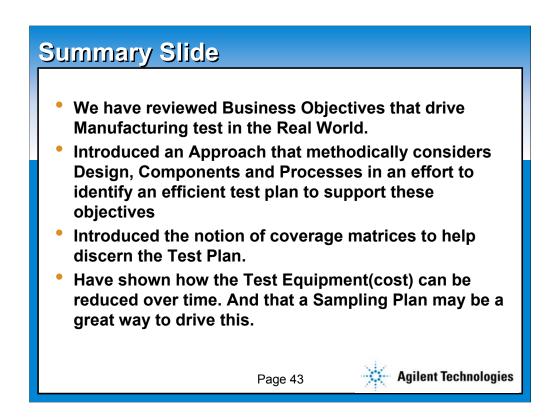
Now that we have moved through all the filters in our approach it is time to summarize our findings. We can do this through another matrix similar to the one introduced for the supply chain. Here we can get an instant view of what form our test plan should take. We note that the bottom half here (in a fictitious Bluetooth IC implementation) almost totally drops out---that is the good news. There are a number of conclusions drawn here which are too detailed to go into right now. But we can see how we should start (with all the A's and C's) and then drive to only the A's. We find that the supply chain column (IC test) provides some excellent coverage in this case.





## Solutions over Time





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